REMARKS

Claims 1, 6, 11, 13-16, 18-20, and 21-25 are currently amended. Applicant contends that the amendments contained herein are supported by the Specification as filed and thus do not constitute new matter.

Claim Objections

Claims 11 and 23, as currently amended, overcome the informalities noted in the Office Action.

Rejections Under 35 U. S. C. § 112

Claims 1-27 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, in paragraph (a), the Examiner asserted that throughout claims 1-27 are recited terms such as "copying," "reading," or "writing" with no explanation of what is doing these things.

Applicant respectfully submits that claims 1-10 are apparatus claims and no "copying," "reading," or "writing" is occurring. Therefore, claims 1-10 are not indefinite and distinctly claim the subject matter that Applicant regards as the invention with regard to "copying," "reading," or "writing." Therefore, the rejection of claims 1-10 should be removed.

Claims 11, 16, 21, 23, and 25, as currently amended, overcome the rejections thereof under 35 U.S.C. § 112, second paragraph. Claims 12-15, claims 17-20, claim 22, claim 24, and claims 26-27, respectively depend from claims 11, 16, 21, 23, and 25 and should be allowed under 35 U.S.C. § 112, second paragraph as originally written or as currently amended to conform to their respective currently amended base claim.

Claims 1 and 6, as currently amended, overcome the rejections thereof in paragraphs (b) and (c), respectively.

Rejections Under 35 U.S.C. § 102

Claims 1-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Arasawa et al. (JP Patent 08221312 A1). Claims 1-27 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Pashley et al. (U.S. Patent 6,418,506). Applicant reserves the right to swear behind Pashley et al. Claims 1-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Schumann et al. (U.S. Patent 5,732,017). Applicant respectfully traverses these rejections.

Each of claims 1 and 6, as currently amended, includes an array of non-volatile memory cells arranged in a plurality of addressable banks and a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, where each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks.

Applicant carefully reviewed a certified translation of Arasawa et al. (submitted herewith) and found no indication of bank buffers and addressable banks coupled one to one, as in each of claims 1 and 6. Instead, Figure 1 of Arasawa et al. shows data buffers 7(1) and 7(2) coupled to a buffer switch circuit 12 that is coupled to an access controller 6 that is coupled to flash-type EEPROMs 2(1), 2(2), and 2(3). Moreover, the buffers of Arasawa et al. are not adapted to store data from a row of memory cells. Rather, Arasawa et al. writes from data buffers 7 to EEPROMs 2, as described in paragraphs [0015], [0016], and [0018]. Therefore, Arasawa et al. does not include each and every element of each of claims 1 and 6, and claims 1 and 6 should be allowed over Arasawa et al.

Applicant carefully reviewed Pashley et al. and Schumann et al. and found no indication of an array of non-volatile memory cells arranged in a plurality of addressable banks and a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, as in each of claims 1 and 6. Pashley et al. has an interface 102 coupled to a *single* RAM write buffer array 101 and a *single* flash array 103 (Figure 1 and column 3, lines 39-40). Schumann et al. has a flash memory array 11 and an EEPROM array 13 that share I/O buffer circuitry 19 (see Figure 1 and column3, lines 53-58). Schumann et

al. has address buffers 25, 27, and 29 (see Figure 1 and column 4, lines 7-8) that are not adapted to store data from memory arrays 11 and 13, as do the buffers of each of claims 1 and 6. Schumann et al. has data latches 23 and 39 (see Figure 1 and column 5, lines 26-28) respectively connected to memory arrays 11 and 13 that are not adapted to store data from memory arrays 11 and 13. Therefore, neither Pashley et al. nor Schumann et al. includes each and every element of each of claims 1 and 6, and claims 1 and 6 should be allowed over Pashley et al. and Schumann et al.

Claims 2-5 depend directly or indirectly from claim 1 and thus include patentable limitations of claim 1. Claims 7-10 depend directly or indirectly from claim 6 and thus include patentable limitations of claim 6. Therefore, claims 2-5 and claims 7-10 should be allowed.

Claim 11, as currently amended, includes copying first data stored in a row of a first non-volatile memory cell array bank to a first buffer circuit using control circuitry of the memory, copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit using the control circuitry, performing a write operation to write third data to the first array bank using a first external processor coupled to the flash memory, reading the first data from the first buffer circuit using the first processor while performing the write operation, and reading the second data from the second array bank using a second external processor coupled to the flash memory while performing the write operation.

Neither Arasawa et al., Pashley et al., nor Schumann et al. includes copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit and reading the second data from the second array bank using a second external processor coupled to the flash memory while performing a write operation to write third data to a first array bank using a first external processor. Therefore, neither Arasawa et al., Pashley et al., nor Schumann et al. includes each and every element of claim 11, and claim 11 should be allowed.

Claims 12-15 depend directly or indirectly from claim 11 and thus include patentable limitations of claim 11. Therefore, claims 12-15 should be allowed.

Claim 16, as currently amended, includes copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the memory, performing a write operation to write second data to the first array bank using an external processor coupled to the flash memory in response to the external processor, reading the first data from the buffer circuit using the processor while performing the write operation, wherein the first data contains instruction code for the processor, and monitoring the write operation with the processor in response to the instruction code.

Neither Arasawa et al. nor Pashley et al. includes copying first data stored in a row of a first array bank to a buffer circuit and monitoring a write operation with a processor in response to an instruction code contained in the first data, as in claim 16. Schumann et al. concurrently reads program instruction codes from a flash memory 11 through an input/output buffer 19 and writes data to a *separate* EEPROM memory 13 (see Figure 1, column 3, lines 39-44, column 5, lines 20-30, and column 6, lines 43-44). However, there is no indication of copying first data stored in a row of a *first array bank* that contains instruction code for a processor to a buffer circuit and reading the first data from the buffer circuit while writing second data to the *first array bank*, as in claim 16. Therefore, neither Arasawa et al., Pashley et al., nor Schumann et al. includes each and every element of claim 16, and claim 16 should be allowed.

Claims 17-20 depend directly from claim 16 and thus include patentable limitations of claim 16. Moreover, claim 18 provides for reading third data from a second array bank with a second external processor while performing the write operation of claim 16. There is no indication of this in Arasawa et al., Pashley et al., or Schumann et al. Therefore, claims 17-20 should be allowed.

Each of claims 21 and 23, as currently amended, include copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the memory in response to a command from an external processor coupled to the flash memory, performing a write operation to write second data to a second row of the first array bank using the processor in response to a write command provided by the processor, reading the first data from the buffer circuit using the processor while performing the write

operation in response to a read command provided by the processor, wherein the first data contains instruction code for the processor, and monitoring a status register of the flash memory with the processor in response to the instruction code.

Neither Arasawa et al. nor Pashley et al. includes copying first data stored in a first row of a first array bank to a buffer circuit and monitoring a status register of the flash memory with a processor in response to an instruction code contained in the first data, as in each of claims 21 and 23. Schumann et al. concurrently reads program instruction codes from a flash memory 11 through an input/output buffer 19 and writes data to a *separate* EEPROM memory 13 (see Figure 1, column 3, lines 39-44, column 5, lines 20-30, and column 6, lines 43-44). However, there is no indication of copying first data stored in a first row of a *first array bank* that contains instruction code for a processor to a buffer circuit and reading the first data from the buffer circuit while writing second data to a second row of the *first array bank*, as in each of claims 21 and 23. Therefore, neither Arasawa et al., Pashley et al., nor Schumann et al. includes each and every element of each of claims 21 and 23, and claims 21 and 23 should be allowed.

Claim 22 depends directly from claim 21 and thus includes patentable limitations of claim 21. Moreover, claim 22 provides for reading third data from a second array bank with a second external processor while performing the write operation of claim 21. There is no indication of this in Arasawa et al., Pashley et al., or Schumann et al. Claim 24 depends directly from claim 23 and thus includes patentable limitations of claim 23. Moreover, claim 24 provides for reading third data from a second array bank with a second external processor while performing the write operation of claim 23. There is no indication of this in Arasawa et al., Pashley et al., or Schumann et al. Therefore, claims 22 and 24 should be allowed.

Claim 25, as currently amended, includes storing instruction code in each of a plurality of array blocks of the synchronous flash memory, and copying the instruction code from a first array block to a buffer circuit using control circuitry of the memory during a write operation to the first array block using an external processor coupled to the

memory so that the instruction code can be read from the buffer circuit using the external processor during the write operation.

Neither Arasawa et al. nor Pashley et al. includes storing instruction code in each of a plurality of array blocks of the synchronous flash memory, and copying the instruction code from a first array block to a buffer circuit using control circuitry of the memory during a write operation to the first array block using an external processor coupled to the memory so that the instruction code can be read from the buffer circuit using the external processor during the write operation, as in claim 25. Schumann et al. concurrently reads program instruction codes from a flash memory 11 through an input/output buffer 19 and writes data to a *separate* EEPROM memory 13 (see Figure 1, column 3, lines 39-44, column 5, lines 20-30, and column 6, lines 43-44). However, there is no indication of copying the instruction code from a *first* array block to a buffer circuit during a write operation to the *first* array block using an external processor coupled to the memory so that the instruction code can be read from the buffer circuit using the external processor during the write operation, as in claim 25. Therefore, neither Arasawa et al., Pashley et al., nor Schumann et al. includes each and every element of claim 25, and claim 25 should be allowed.

Claims 26-27 depend directly from claim 25 and thus include patentable limitations of claim 25. Therefore, claim 25 should be allowed.

Double Patenting Rejection

The Examiner provisionally rejected claims 1-27 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of co-pending U. S. Patent Application Serial No. 09/628,184 (the '184 application). Applicant respectfully traverses this rejection.

Claims 1-27 of the present application include writing to an array bank while reading data from a buffer connected to the array bank, where the data has been copied from the array bank to the buffer. In contrast, claims 1-23 of the '184 application include writing first data to one bank of a plurality of addressable banks of an array of non-volatile memory cells and simultaneously reading second data from another bank of the

plurality of addressable banks of the array of non-volatile memory cells. Therefore, claims 1-27 of the present application are patentably distinct from claims 1-23 of the '184 application because claims 1-27 of the present application require non-obvious limitations not included in claims 1-23 of the '184 application. Therefore, the rejection of claims 1-27 under the judicially created doctrine of obviousness-type double patenting should be removed, and claims 1-27 should be allowed.

CONCLUSION

Claims 1, 6, 11, 13-16, 18-20, and 21-25 are currently amended. In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. No new matter has been added and no additional fee is required by this amendment and response.

The Examiner is invited to contact Applicant's representative at the number below if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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